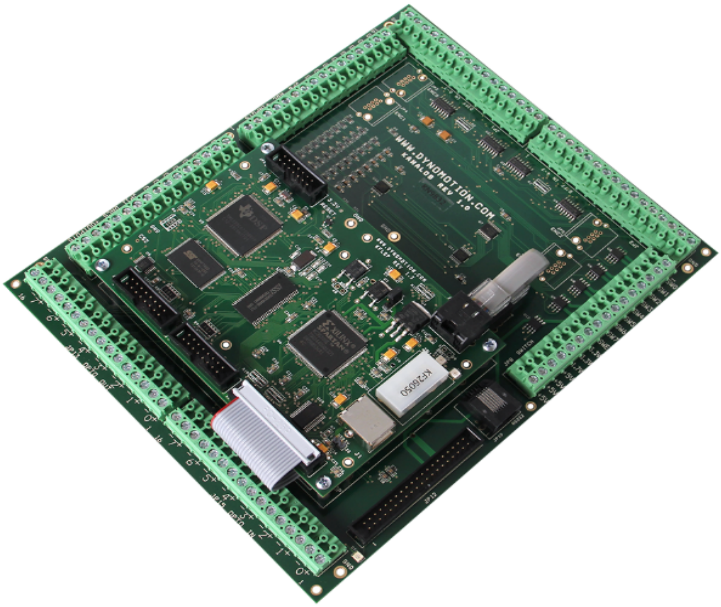
Kanalog Expansion Board for KFLOP

User Manual



Using Kanalog 1.0

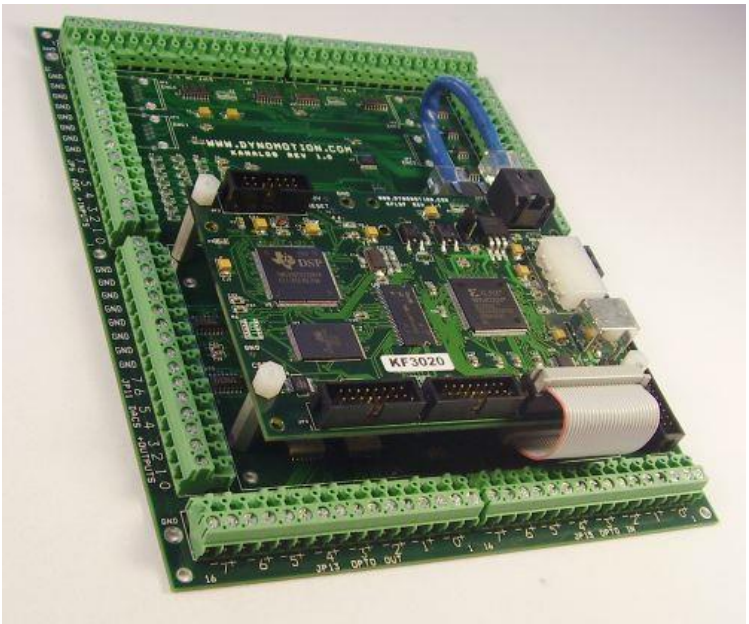
Kanalog adds Analog and Digital I/O to Dynomotion's *KFLOP* motion controller.

Kanalog provides 6 types of various I/O which is enough to completely drive many types of machine tools.

Standard +/-10V Analog outputs may be used to drive Analog Motor Drives. The Analog outputs are true 12 bit DACS, *not* filtered PWMs that have slow response and ripple. All (8) Analog inputs and (8) Analog outputs are all updated every Servo Sample time of 90us (11KHz).

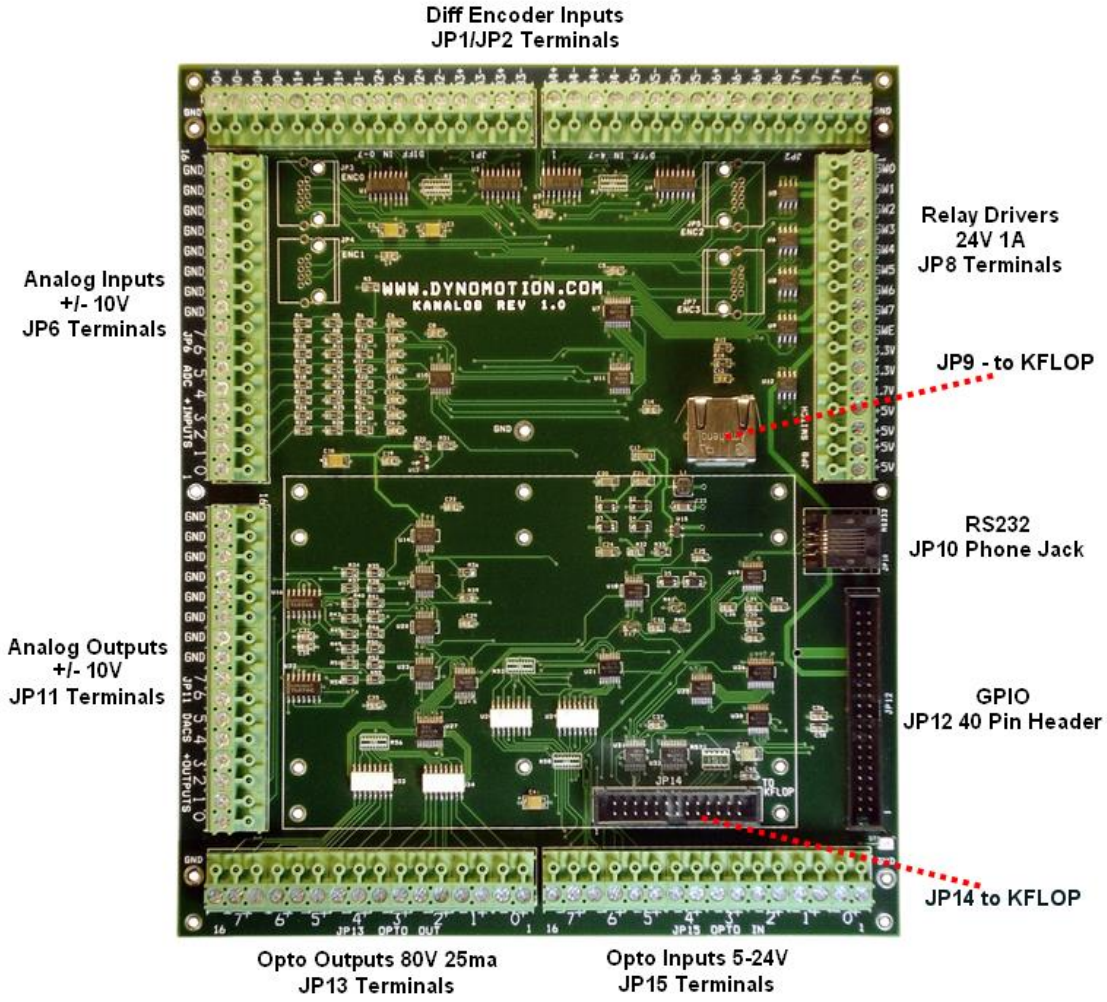
Relay Drivers, Opto Inputs, Opto Outputs, Differential Encoder Inputs, LVTTL inputs and outputs are all included along with 112 screw terminals.

The photo below shows Kanalog with KFlop mounted and two cables that connect the two boards.



Kanalog + KFLOP

Connector Pinouts:



JP1/JP2 Differential Inputs

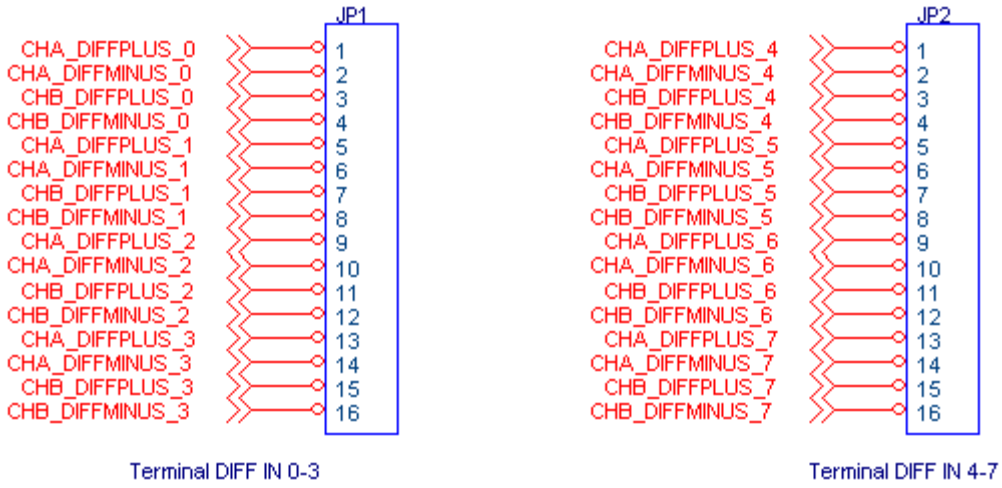
16 Differential Receiver Inputs are provided. Kanalog converts the differential signals to signal ended LVTTL signals and passes them through to existing KFlop I/O pins.

JP1 converts 8 of the signals and connects them to Kflop I/O bits 0-7 (Kflop JP7 Pins 7-14) which are Kflop's 4 encoder A/B input channels.

JP2 converts 8 of the signals and connects them to Kflop I/O bits 36-43 (Kflop JP5 Pins 1-8) which are General Purpose I/O pins.

Typically up to 4 encoder's A/B signals are connected to JP1 and any Z index inputs are connected to JP2

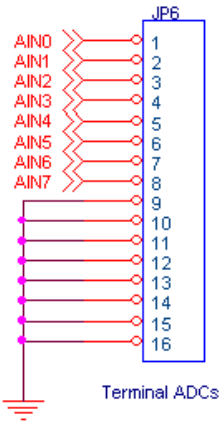
These differential inputs are moderately damped with an internal 470ohm resistor connected across the + to - inputs. If additional termination is required an external resistor may be connected.



JP6 - Analog Inputs +/- 10V

(8) +/- 10V analog inputs are provided. These are mapped and referenced as ADC inputs 0-7 for Kflop configuration purposes. Input impedance is approximately 100K ohms.

(8) ground terminals are provided. Kanalog contains a single solid ground plane so these grounds may be used as any digital or analog ground connection.



JP8 - FET Switch Outputs (relay drivers) - watchdog - power outputs

(8) 24V @ 1Amp relay FET Switch Outputs are available on Kanalog mapped as Output Bits 152-159. When activated (checked on or with state "1") the FET Switches make a connection to ground. Normally a load, such as a relay coil is connected between some appropriate +supply and a Switch input. Therefore when the Switch makes a connection to ground, the load is energized.

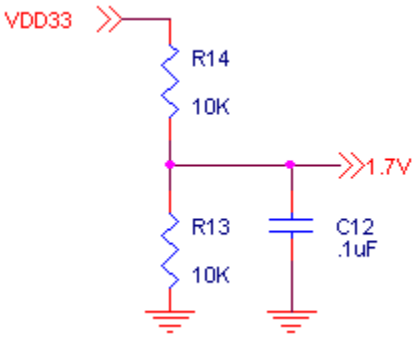
Caution! Inductive loads MUST have a reverse diode connected in parallel with the load to avoid a high voltage spark when the switch opens. Failure to allow a re-circulating current path on any inductive coil such as a relay, solenoid, or motor is likely to cause permanent damage.

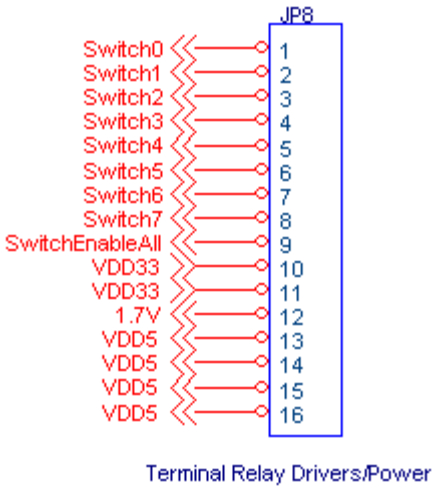
One Enable or Watchdog FET Switch Output is also available (24V @ 1Amp). This switch conducts after Kflop boots, enables the +/-15V generator, and begins communicating with the board. It is recommended that this switch output is used in one of the conditions to enable main system power for motors and other devices.

(2) +3.3V outputs are available to power low current (<100ma) external circuitry.

One low current 1.7V bias current is available. See circuit below:

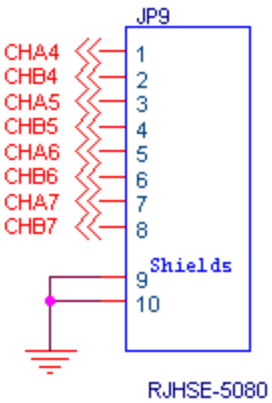
(4) +5V outputs are available to power low current (<100ma) external circuitry such as encoders. Normally +5V is applied to Kflop JR1 (4 pin white Molex connector) and passes through the ribbon connector to Kanalog. However it is also possible to feed +5V into the system via these terminals. If +5V power is fed into both Kflop and Kanalog the exact same +5V supply must be connected to both.





P9 - Differential Signals 8-15 to Kflop

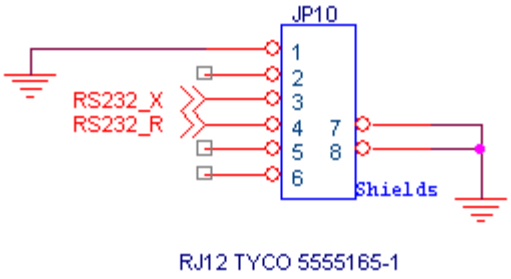
The second (8) of the 16 Differential signals pass through to KFlop through this connector. If only the first 8 differential are used then this connector is not required and the 8 Kflop inputs may be used for some other purpose.



JP10 - RS232

The JP10 6-pin phone connector provides 3-wire RS232 connectivity. JP10 Pin3 is used for transmit data from Kanalog. JP10 Pin 4 is used for receive data going into Kanalog. Receive data is converted to LVTTL and routed to a Kflop I/O bit #44. Data from LVTTL Kflop I/O bit #45 is passed through the RS232 driver and out the Transmit pin. This phone plug connector is designed to be compatible with Automation Direct's PLC line using a crossover phone cable.

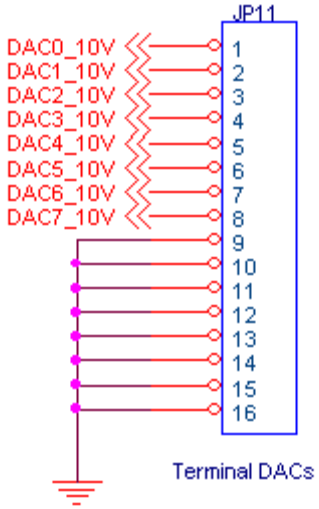
Note: Our pin out numbering may differ from most standards. Pin 1 on the board is the pin closest to JP8.



JP11 - Analog Ouputs +/- 10V

(8) +/- 10V analog ouputs are provided. These are mapped and referenced as DAC outputs 0-7 for Kflop configuration purposes. Output impedance is approximately 2K ohms.

(8) ground terminals are provided. Kanalog contains a single solid ground plane so these grounds may be used as any digital or analog ground connection.



JP12 - General Purpose Inputs, Outputs, Low level analog in, Supplies

JP12 is a standard 40 pin IDC header connector.

(8) 3.3V LVTTL Inputs are provided (SDIN0 - SDIN7) mapped as Kanalog Input bits #128-135. Inputs are diode clamped to 3.3V.

Note: To connect 5V signals a 200ohm external series resistor is required.

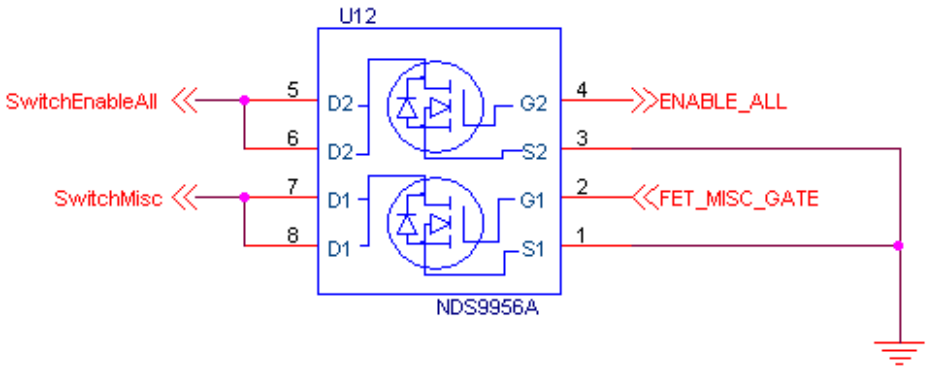
(8) 3.3V LVTTL Outputs are provided (OUT 0 - OUT_7) mapped as Kanalog Output bits #160-167.

ADC channels 0-3 have internal low voltage inputs exposed as signals IN0-IN3. Instead of driving the normal terminal inputs with a voltage range of +/- 10V. The INx pins may be driven with low voltage (0V - 3V) signals with an input impedance of ~10K ohms. This may allow higher resolution with low voltage signals. Caution should be used as these are low voltage unprotected signal inputs.

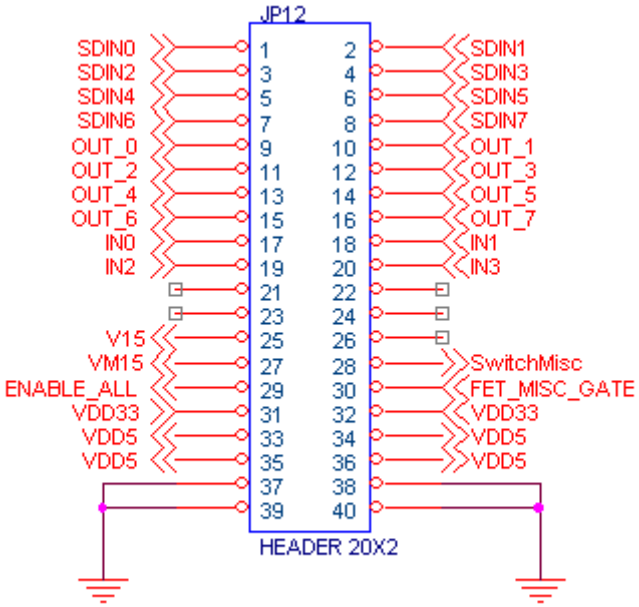
+/- 15V from the internal DC-DC generator is available on pins V15 (+15V) and VM15 (-15V). 70ma is available for external use for each supply.

ENABLE_ALL is the LVTTL equivalent of the SwitchEnableAll FET output if a logic level is desired instead of the FET SWITCH output.

One additional 24V 1Amp FET switch is available with an exposed gate. Drive signal FET_MISC_GATE to 3.3v to turn on the FET (SwitchMisc) output.



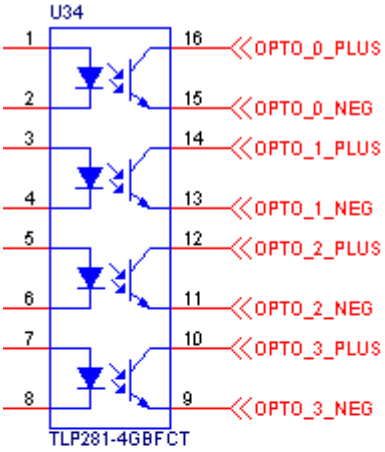
+3.3V and +5V are available on this connector. +3.3V is available as an output only (regulated down from the +5V). +5V is common to all other +5V signals and may be used as input or output.

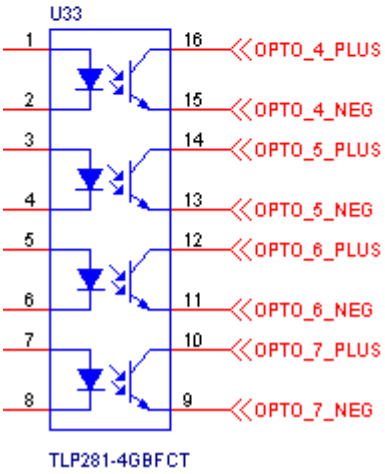


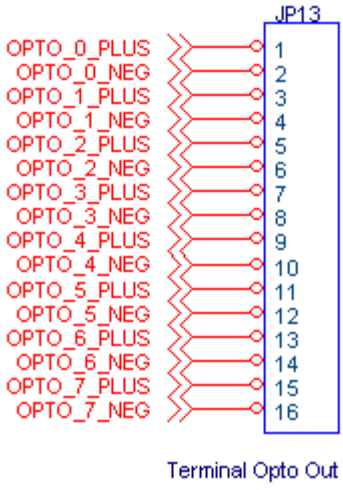
JP13 - Opto Outputs

(8) totaly isolated and independent optically isolated outputs are provided.

Opto output transistors are rated for a max voltage of 80V and will conduct up to 25ma of current.





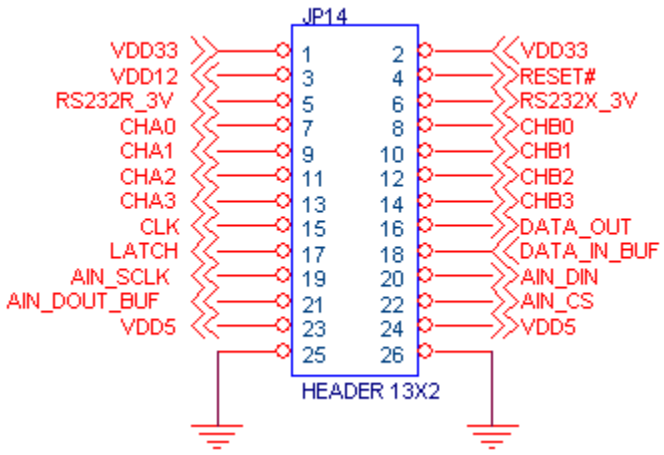


JP14 - Kflop

This is the main connection between Kflop and Kanalog and should consist of a short 26-pin one-one ribbon cable.

Analog and digital data passes through this cable in serial form. The first 8 differential signals pass to the Kflop in parallel form.

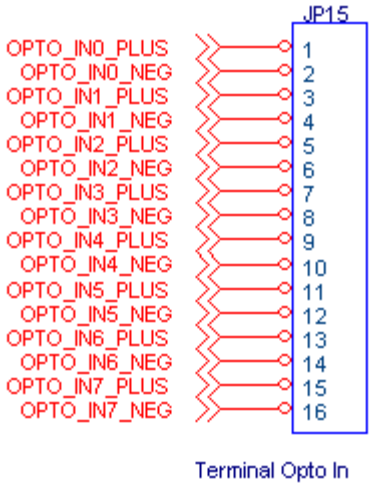
None of these signals should be used by the User.



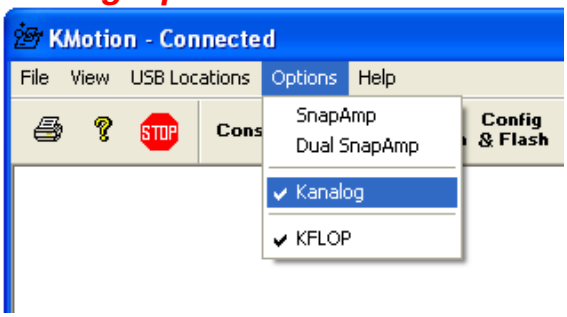
JP15 - Opto Intputs

(8) totaly isolated and independent optically isolated inputs are provided.

Input LEDs have a series resistance of 10Kohms and may be driven directly by any voltage from 5-24V. Max drain of 2.4ma when driven with 24V.



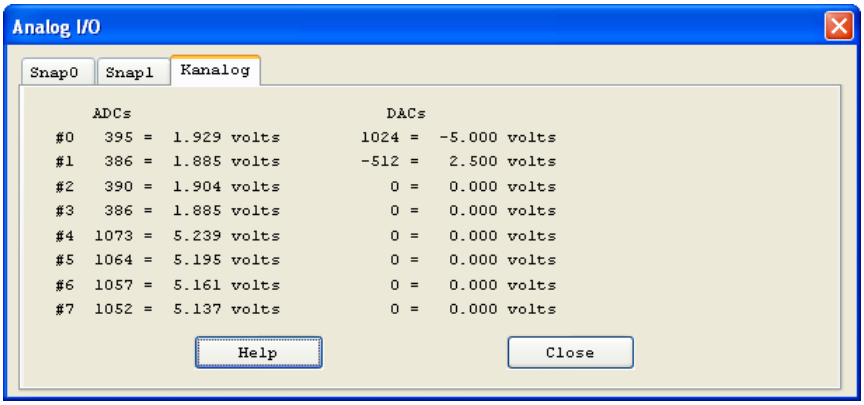
Setting Options



Set options on the KMotion Executive Program for both Kanalog and the required KFlop.

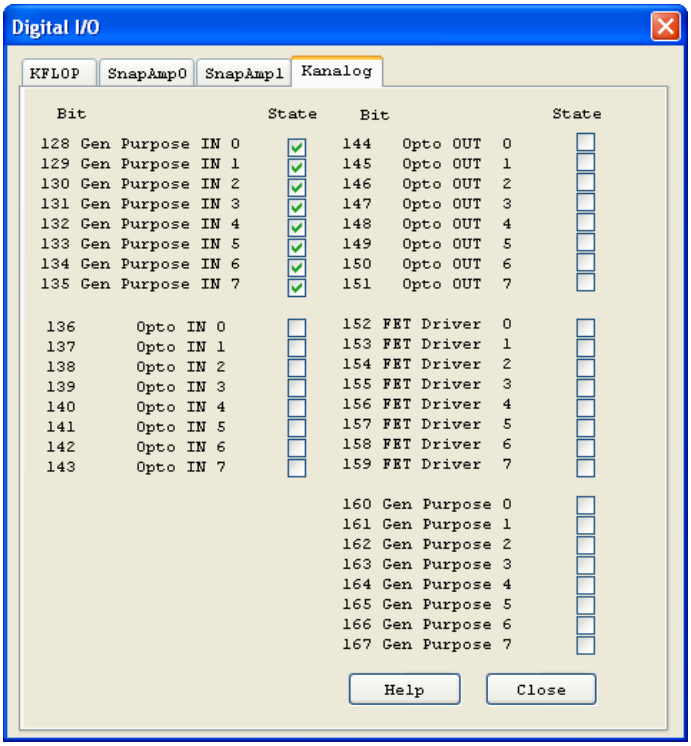
Analog Status

All of the Analog ADC readings and DAC settings can be observed by selecting the Kanalog Tab of the Analog I/O Screen.



Digital Status

All of the Digital I/O can be observed by selecting the Kanalog Tab of the Digital I/O Screen.
Inputs are all on the left side of the screen and Outputs are on the right. Outputs may be toggled by clicking on the state.



Example Configuration

The example configuration below shows a typical configuration where an external analog motor amplifier is to be used with differential encoder feedback and optically isolated limit switches.

Note the areas on the screen circled in red.

The Axis input type has been selected as "Encoder" with the first Input channel set to 0 (Encoders only use one input channel). A differential encoder should then be connected to Kanalog JP1 A0+ A0- B0+ B0-.

The Axis Output type has been selected as "DAC Servo" with the first Output channel set to 0 (DAC Servos only use one output channel). The Motor's Amplifier should then be connected to Kanalog DAC0 JP11 pin 1 (and ground).

Limit Switch Options have selected I/O bits 136 and 137 which are Kanalog Opto Inputs 0 and 1 on JP15 across pins 1&2 and 3&4.